High Speed, Low Noise Video Op Amp

AD829

FEATURES

High Speed
- 120 MHz Bandwidth, Gain = –1
- 230 V/μs Slew Rate
- 90 ns Settling Time to 0.1%

Ideal for Video Applications
- 0.02% Differential Gain
- 0.04° Differential Phase

Low Noise
- 1.7 nV/√Hz Input Voltage Noise
- 1.5 pA/√Hz Input Current Noise

Excellent DC Precision
- 1 mV Max Input Offset Voltage (Over Temp)
- 0.3 mV/°C Input Offset Drift

Flexible Operation
- Specified for ±5 V to ±15 V Operation
- ±3 V Output Swing into a 150 Ω Load
- External Compensation for Gains 1 to 20
- 5 mA Supply Current

Available in Tape and Reel in Accordance with EIA-481A Standard

GENERAL DESCRIPTION

The AD829 is a low noise (1.7 nV/√Hz), high speed op amp with custom compensation that provides the user with gains of ±1 to ±20 while maintaining a bandwidth greater than 50 MHz. The AD829's 0.04° differential phase and 0.02% differential gain performance at 3.58 MHz and 4.43 MHz, driving reverse-terminated 50 Ω or 75 Ω cables, makes it ideally suited for professional video applications. The AD829 achieves its 230 V/μs uncompensated slew rate and 750 MHz gain bandwidth while requiring only 5 mA of current from power supplies.

The AD829's external compensation pin gives it exceptional versatility. For example, compensation can be selected to optimize the bandwidth for a given load and power supply voltage. As a gain-of-two line driver, the –3 dB bandwidth can be increased to 95 MHz at the expense of 1 dB of peaking. The AD829's output can also be clamped at its external compensation pin.

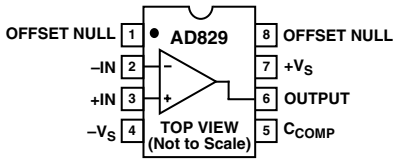
The AD829 exhibits excellent dc performance. It offers a minimum open-loop gain of 30 V/mV into loads as low as 500 Ω, low input voltage noise of 1.7 nV/√Hz, and a low input offset voltage of 1 mV maximum. Common-mode rejection and power supply rejection ratios are both 120 dB.

This op amp is also useful in multichannel, high speed data conversion where its fast (90 ns to 0.1%) settling time is important. In such applications, the AD829 serves as an input buffer for 8-bit to 10-bit A/D converters and as an output I/V converter for high speed DACs.

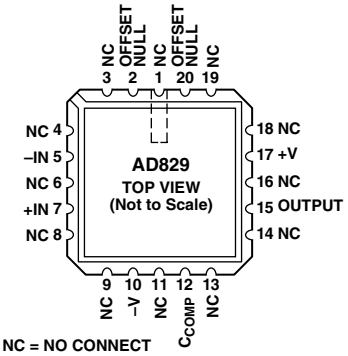
CONNECTION DIAGRAMS

8-Lead

PDIP(N), Cerdip (Q), and SOIC (R) Packages



20-Lead LCC Pinout



NC = NO CONNECT

Operating as a traditional voltage feedback amplifier, the AD829 provides many of the advantages a transimpedance amplifier offers. A bandwidth greater than 50 MHz can be maintained for a range of gains through the replacement of the external compensation capacitor. The AD829 and the transimpedance amplifier are both unity gain stable and provide similar voltage noise performance (1.7 nV/√Hz); however, the current noise of the AD829 (1.5 pA/√Hz) is less than 10% of the noise of transimpedance amps. The inputs of the AD829 are symmetrical.

PRODUCT HIGHLIGHTS

1. Input voltage noise of 2 nV/√Hz, current noise of 1.5 pA/√Hz, and 50 MHz bandwidth, for gains of 1 to 20, make the AD829 an ideal preamp.
2. Differential phase error of 0.04° and a 0.02% differential gain error, at the 3.58 MHz NTSC and 4.43 MHz PAL and SECAM color subcarrier frequencies, make the op amp an outstanding video performer for driving reverse-terminated 50 Ω and 75 Ω cables to ±1 V (at their terminated end).
3. The AD829 can drive heavy capacitive loads.
4. Performance is fully specified for operation from ±5 V to ±15 V supplies.
5. The AD829 is available in plastic, CERDIP, and small outline packages. Chips and MIL-STD-883B parts are also available. The SOIC-8 package is available for the extended temperature range of –40°C to +125°C.

AD829—SPECIFICATIONS (@ T_A = 25°C and V_S = ±15 V dc, unless otherwise noted.)

Model	Conditions	V_S	AD829JR Min	AD829JR Typ	AD829JR Max	AD829AR Min	AD829AR Typ	AD829AR Max	AD829AQ/S Min	AD829AQ/S Typ	AD829AQ/S Max	Unit
INPUT OFFSET VOLTAGE		±5 V, ±15 V		0.2	1		0.2	1		0.1	0.5	mV
	T_{MIN} to T_{MAX}				1			1			0.5	mV
Offset Voltage Drift		±5 V, ±15 V		0.3			0.3			0.3		µV/°C
INPUT BIAS CURRENT		±5 V, ±15 V		3.3	7		3.3	7		3.3	7	µA
	T_{MIN} to T_{MAX}				8.2			9.5			9.5	µA
INPUT OFFSET CURRENT		±5 V, ±15 V		50	500		50	500		50	500	nA
	T_{MIN} to T_{MAX}				500			500			500	nA
Offset Current Drift		±5 V, ±15 V		0.5			0.5			0.5		nA/°C
OPEN-LOOP GAIN	V_O = ±2.5 V	±5 V										
	R_{LOAD} = 500 Ω		30	65		30	65		30	65		V/mV
	T_{MIN} to T_{MAX}		20			20			20			V/mV
	R_{LOAD} = 150 Ω			40			40			40		V/mV
	V_{OUT} = ±10 V	±15 V										
	R_{LOAD} = 1 kΩ		50	100		50	100		50	100		V/mV
	T_{MIN} to T_{MAX}		20			20			20			V/mV
	R_{LOAD} = 500 Ω			85			85			85		V/mV
DYNAMIC PERFORMANCE												
Gain Bandwidth Product		±5 V		600			600			600		MHz
		±15 V		750			750			750		MHz
Full Power Bandwidth[1, 2]	V_O = 2 V p-p											
	R_{LOAD} = 500 Ω	±5 V		25			25			25		MHz
	V_O = 20 V p-p											
	R_{LOAD} = 1 kΩ	±15 V		3.6			3.6			3.6		MHz
Slew Rate[2]	R_{LOAD} = 500 Ω	±5 V		150			150			150		V/µs
	R_{LOAD} = 1 kΩ	±15 V		230			230			230		V/µs
Settling Time to 0.1%	A_V = –19											
	–2.5 V to +2.5 V	±5 V		65			65			65		ns
	10 V Step	±15 V		90			90			90		ns
Phase Margin[2]	C_{LOAD} = 10 pF	±15 V										
	R_{LOAD} = 1 kΩ			60			60			60		Degrees
DIFFERENTIAL GAIN ERROR[3]	R_{LOAD} = 100 Ω	±15 V										
	C_{COMP} = 30 pF			0.02			0.02			0.02		%
DIFFERENTIAL PHASE ERROR[3]	R_{LOAD} = 100 Ω	±15 V										
	C_{COMP} = 30 pF			0.04			0.04			0.04		Degrees
COMMON-MODE REJECTION	V_{CM} = ±2.5 V	±5 V	100	120		100	120		100	120		dB
	V_{CM} = ±12 V	±15 V	100	120		100	120		100	120		dB
	T_{MIN} to T_{MAX}		96			96			96			dB
POWER SUPPLY REJECTION	V_S = ±4.5 V to ±18 V		98	120		98	120		98	120		dB
	T_{MIN} to T_{MAX}		94			94			94			dB
INPUT VOLTAGE NOISE	f = 1 kHz	±15 V		1.7	2		1.7	2		1.7	2	nV/√Hz
INPUT CURRENT NOISE	f = 1 kHz	±15 V		1.5			1.5			1.5		pA/√Hz
INPUT COMMON-MODE VOLTAGE RANGE		±5 V		+4.3			+4.3			+4.3		V
				–3.8			–3.8			–3.8		V
		±15 V		+14.3			+14.3			+14.3		V
				–13.8			–13.8			–13.8		V
OUTPUT VOLTAGE SWING	R_{LOAD} = 500 Ω	±5 V	±3.0	±3.6		±3.0	±3.6		±3.0	±3.6		V
	R_{LOAD} = 150 Ω	±5 V	±2.5	±3.0		±2.5	±3.0		±2.5	±3.0		V
	R_{LOAD} = 50 Ω	±5 V		±1.4			±1.4			±1.4		V
	R_{LOAD} = 1 kΩ	±15 V	±12	±13.3		±12	±13.3		±12	±13.3		V
	R_{LOAD} = 500 Ω	±15 V	±10	±12.2		±10	±12.2		±10	±12.2		V
Short Circuit Current		±5 V, ±15 V		32			32			32		mA
INPUT CHARACTERISTICS												
Input Resistance (Differential)				13			13			13		kΩ
Input Capacitance (Differential)[4]				5			5			5		pF
Input Capacitance (Common Mode)				1.5			1.5			1.5		pF
CLOSED-LOOP OUTPUT RESISTANCE	A_V = +1, f = 1 kHz			2			2			2		mΩ

Model	Conditions	V_S	AD829JR Min	AD829JR Typ	AD829JR Max	AD829AR Min	AD829AR Typ	AD829AR Max	AD829AQ/S Min	AD829AQ/S Typ	AD829AQ/S Max	Unit
POWER SUPPLY												
Operating Range			±4.5		±18	±4.5		±18	±4.5		±18	V
Quiescent Current		±15 V		5	6.5		5	6.5		5	6.5	mA
	T_{MIN} to T_{MAX}				8.0			8.0			8.2/8.7	mA
		±15 V		5.3	6.8		5.3	6.8		5.3	6.8	mA
	T_{MIN} to T_{MAX}				8.3			9.0			8.5/9.0	mA
TRANSISTOR COUNT	Number of Transistors			46			46			46		

NOTES
[1]Full Power Bandwidth = Slew Rate/2 π V_{PEAK}.
[2]Tested at Gain = +20, C_{COMP} = 0 pF.
[3]3.58 MHz (NTSC) and 4.43 MHz (PAL and SECAM).
[4]Differential input capacitance consists of 1.5 pF package capacitance plus 3.5 pF from the input differential pair.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	±18 V
Internal Power Dissipation[2]	
PDIP (N)	1.3 W
SOIC (R)	0.9 W
CERDIP (Q)	1.3 W
LCC (E)	0.8 W
Input Voltage	±V
Differential Input Voltage[3]	±6 V
Output Short Circuit Duration	Indefinite
Storage Temperature Range (Q, E)	–65°C to +150°C
Storage Temperature Range (N, R)	–65°C to +125°C
Operating Temperature Range	
AD829J	0°C to 70°C
AD829A	–40°C to +125°C
AD829S	–55°C to +125°C
Lead Temperature Range (Soldering 60 sec)	300°C

NOTES

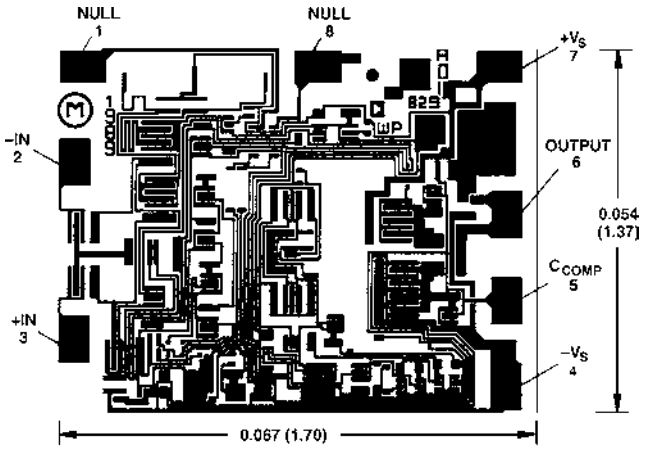
[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; the functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2] Maximum internal power dissipation is specified so that T_J does not exceed 150°C at an ambient temperature of 25°C.
Thermal characteristics:
8-lead PDIP package: θ_{JA} = 100°C/W (derate at 8.7 mW/°C)
8-lead CERDIP package: θ_{JA} = 110°C/W (derate at 8.7 mW/°C)
20-lead LCC package: θ_{JA} = 77°C/W
8-lead SOIC package: θ_{JA} = 125°C/W (derate at 6 mW/°C).

[3] If the differential voltage exceeds 6 V, external series protection resistors should be added to limit the input current.

METALLIZATION PHOTO

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



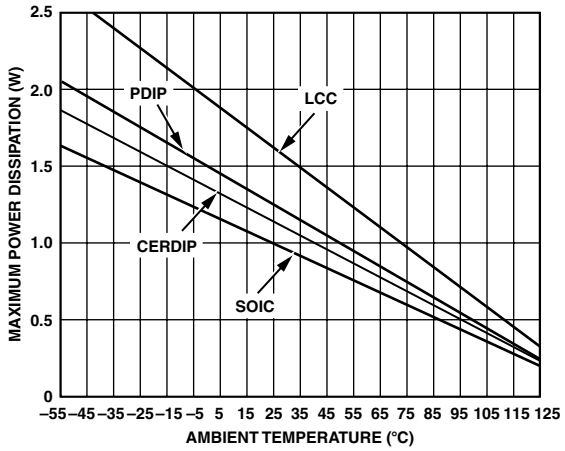


Figure 1. Maximum Power Dissipation vs. Temperature

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD829 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

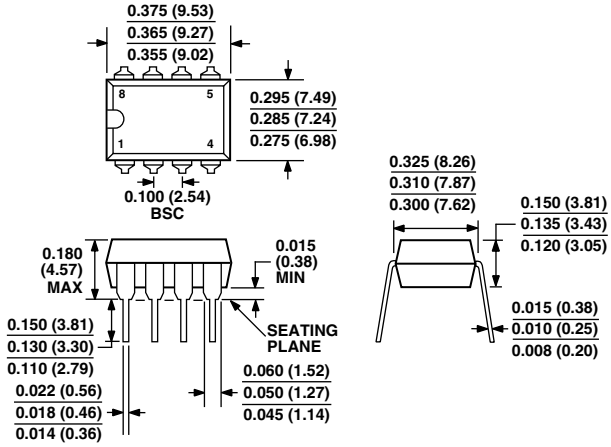
Model	Temperature Range	Package Description	Package Option
AD829AR	–40°C to +125°C	8-Lead Plastic SOIC	R-8
AD829AR-REEL	–40°C to +125°C	8-Lead Plastic SOIC	R-8
AD829AR-REEL7	–40°C to +125°C	8-Lead Plastic SOIC	R-8
AD829ARZ*	–40°C to +125°C	8-Lead Plastic SOIC	R-8
AD829ARZ-REEL*	–40°C to +125°C	8-Lead Plastic SOIC	R-8
AD829ARZ-REEL7*	–40°C to +125°C	8-Lead Plastic SOIC	R-8
AD829JN	0°C to 70°C	8-Lead Plastic PDIP	N-8
AD829JR	0°C to 70°C	8-Lead Plastic SOIC	R-8
AD829JR-REEL	0°C to 70°C	8-Lead Plastic SOIC	R-8
AD829JR-REEL7	0°C to 70°C	8-Lead Plastic SOIC	R-8
AD829AQ	–40°C to +125°C	8-Lead CERDIP	Q-8
AD829SQ	–55°C to +125°C	8-Lead CERDIP	Q-8
AD829SQ/883B	–55°C to +125°C	8-Lead CERDIP	Q-8
5962-9312901MPA	–55°C to +125°C	8-Lead CERDIP	Q-8
AD829SE/883B	–55°C to +125°C	20-Lead LCC	E-20A
5962-9312901M2A	–55°C to +125°C	20-Lead LCC	E-20A
AD829JCHIPS		Die	
AD829SCHIPS		Die	

*Z = Pb-free part.

OUTLINE DIMENSIONS

8-Lead Plastic Dual In-Line Package [PDIP]
(N-8)

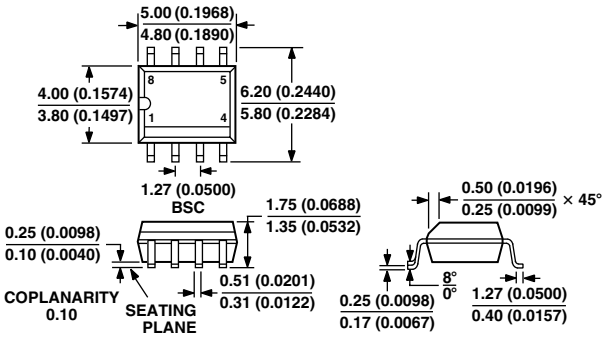
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-095AA
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

8-Lead Standard Small Outline Package [SOIC]
Narrow Body
(R-8)

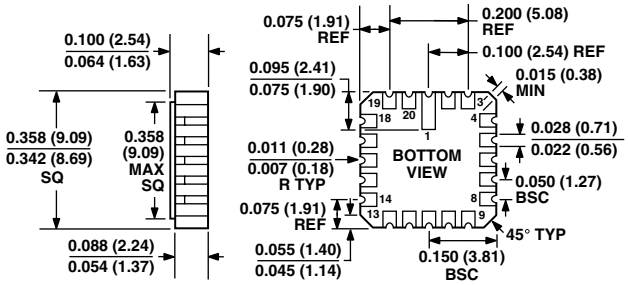
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-012AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

20-Terminal Ceramic Leadless Chip Carrier [LCC]
(E-20A)

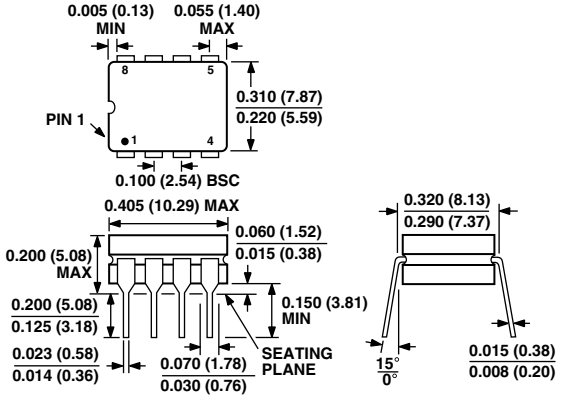
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETERS DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

8-Lead Ceramic Dual In-Line Package [CERDIP]
(Q-8)

Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETERS DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN